REMARKS/ARGUMENTS

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al. (5,578,421). Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (5,578,421) or Tzu et al. (6,001,512) in view of Lee (6,528,836).

1. Rejection of claim 1 under 35 U.S.C. 102(e):

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al. for reasons of record that can be found on page 2 in the Office action identified above.

Response:

Claim 1 has been amended to contain the limitation of "using the PSM to perform a pattern transferring process to transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**". The limitation is fully supported by the specification and by Figures 7-10 for instance. No new matter is introduced.

According to claim 1, a method of forming and testing a PSM, comprising: providing a mask substrate, a surface of the mask substrate comprising a main field region and a blank periphery region surrounding the main field region; forming a first pattern, at least one second pattern and at least one third pattern **within the main field region** to form the PSM; using the PSM to perform a pattern transferring process to transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; and **using the second and third patterns transferred to the circuit region of the semiconductor wafer to perform a PSM test**.

It is an advantage of the present application against the prior art that the first, second

and third patterns are formed in the main field region that corresponds to the circuit region. Therefore, the PSM test is performed by using the second and third patterns transferred to the circuit region of the semiconductor wafer in subsequent processes to more accurately monitor the etching uniformity **within the circuit region** etched by utilizing the PSM. In addition, a registration test, a phase angle test and a transparency test of the PSM are simultaneously performed in a single step. The manufacturing processes are thus simplified, and the production lead-time is reduced as well. Consequently, the production cost is significant saved, making the product more competitive in the market.

Regarding to Hasegawa's disclosure, Hasegawa et al. teach strip patterns 9 and 10 for reducing the light strength, which propagates to the area on wafer under the region 6. Examiner points that Hasegawa et al. teach a pattern forming method, comprising the steps of: exposing a predetermined first area of said substrate 1 by using a photomask including a first portion 5 and a second portion 6, said first portion 5 being an element pattern portion including a semitransparent phase shifting region, and said second portion 6 including a semitransparent phase shifting pattern 9 and a transparent pattern 10. Examiner points that Hasegawa et al. teach two DRAM element areas 5 arranged in a transparent substrate 1. A scribing area 14 is provided between the two pattern element areas 5. In addition, **in a peripheral scribing area 15** on two sides perpendicular to each other, a pattern for measuring the accuracy of the mask alignment, a target pattern for the mask alignment, and the like are arranged, which becomes necessary for the process of manufacturing a device.

However, according to FIG. 2A-FIG. 5A and col. 6 lines 15-21 in Hasegawa's disclosure, the testing patterns are all formed in **scribing areas**. In contrast, the second

pattern and third pattern, which are measured in the PSM test, are formed **within the main field region**, which corresponds to **the circuit region** of the semiconductor wafer in the present application. Because the PSM test is performed by using the second and third patterns in the circuit region, the present application can monitor the etching uniformity **in the circuit region** etched by utilizing the PSM more accurately.

Applicant believes that Hasegawa et al. do not disclose these characteristics of: (1) forming a first pattern, at least one second pattern and at least one third pattern **within the main field region**; (2) transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; and (3) using **the second and third patterns** transferred to the circuit region of the semiconductor wafer to **perform a PSM test**. Since Hasegawa et al. do not disclose the above-mentioned characteristics that are taught in claim 1, the amended claim 1 should be allowable in consideration of 35 U.S.C. 102(e). Reconsideration of claim 1 is respectfully requested.

2. Rejection of claims 1-20 under 35 U.S.C. 103(a):

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. or Tzu et al. in view of Lee for reasons of record, as recited on pages 3-4 of the above-indicated Office action.

Response:

Claim 1 and claim 13 have been amended to contain the limitation of "using the PSM to perform a pattern transferring process to transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**". The limitation is fully supported by the specification and by Figures 7-10 for instance. No new matter is introduced.

According to the amended claim 1, a method of forming and testing a PSM comprising: providing a mask substrate, a surface of the mask substrate comprising a main field region and a blank periphery region surrounding the main field region; forming a first pattern, at least one second pattern and at least one third pattern **within the main field region** to form the PSM; using the PSM to perform a pattern transferring process to transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; and **using the second and third patterns transferred to the circuit region of the semiconductor wafer to perform a PSM test**.

According to the amended claim 13, a method of forming and testing a PSM comprising: providing a mask substrate, a surface of the mask substrate comprising a main field region and **an anti-static charge border region** surrounding the main field region; forming a first pattern and at least one second pattern **within the main field region** to form the PSM; using the PSM to perform a pattern transferring process to transfer the first pattern and the second pattern to **a circuit region of a semiconductor wafer**; and using the second pattern transferred to the circuit region of the semiconductor wafer to **perform a PSM test**.

Regarding to Hasegawa's disclosure, Hasegawa et al. do not disclose the characteristics of (1) forming a first pattern, at least one second pattern and at least one third pattern **within the main field region**; (2) transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; (3) using **the second and third patterns** transferred to the circuit region of the semiconductor wafer to **perform a PSM test**; and (4) a surface of the mask substrate comprising a main field region and **an anti-static charge border region** surrounding the main field region. These characteristics are disclosed in the amended claim 1 and claim 13.

Regarding to Tzu's disclosure, Tzu et al. teach a mask for providing a buffer distance surrounding the features of the test patterns. The buffer distance is free of sub-resolution contact holes 20. When the buffer distance is correctly chosen problems due to side lobe effect at the frame cell portion 16 of the mask are prevented. As shown in Fig. 1-Fig. 10 and col. 3 lines 10-24, the sub-resolution contact holes 20 and **the test patterns** are all form **in the border region 14, which is the scribe line area**.

Accordingly, Tzu et al. do not disclose the characteristics of (1) forming a first pattern, at least one second pattern and at least one third pattern **within the main field region**; (2) transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; (3) using **the second and third patterns** transferred to the circuit region of the semiconductor wafer to **perform a PSM test**; and (4) a surface of the mask substrate comprising a main field region and **an anti-static charge border region** surrounding the main field region. These characteristics are disclosed in the amended claim 1 and claim 13.

Regarding to Lee's disclosure, Lee teaches an active anti-ESD pod for transporting photomask comprises six body portions delimiting the container, an electrically conducting plate on the top portion, and an electrically conducting handle connected to the plate. As shown in Fig. 4, the photomask in lee's disclosure should have an active anti-ESD protection 92 to ensure a dynamic and spontaneous dispatching of an electrostatic charge. It is different from the present application.

Lee does not disclose the characteristics of (1) forming a first pattern, at least one second pattern and at least one third pattern **within the main field region**; (2) transfer the first pattern, the second pattern and the third pattern to **a circuit region of a semiconductor wafer**; and (3) using **the second and third patterns** transferred to the circuit region of the semiconductor wafer to **perform a PSM test**.

In contrast to the cited references, the second and third patterns are formed in the main field region that corresponds to the circuit region. Based on the method of the present application, the PSM test is performed more accurately to monitor the etching uniformity **within the circuit region**. Since Hasegawa et al., Tzu et al. and Lee do not disclose forming a second pattern and a third pattern **within the main field region**, transfer the second pattern and the third pattern to **a circuit region of a semiconductor wafer**, and using **the second and third patterns** transferred to the circuit region to **perform a PSM test**, the combination of Hasegawa's disclosure, Tzu's disclosure and Lee's disclosure do not teach all the limitations of claim 1 and claim 13. Therefore, in comparison with the combination of the cited references, application believes that the amended claim 1 and claim 13 should be allowable in consideration of 35 U.S.C. 103(a). Reconsideration of claim 1 and claim 13 is respectfully requested.

Referring to claim 3 and claim 18, Hasegawa et al., Tzu et al. and Lee do not disclose that the PSM test comprises at least one of a registration test, a phase angle test and a transparency test.

Referring to claim 4 and claim 15, Hasegawa et al., Tzu et al. and Lee do not disclose that the second pattern is positioned on the border of the main field region, and the transferred second pattern on the circuit region of the semiconductor wafer is employed to perform the registration test.

Referring to claim 5 and claim 15, Hasegawa et al., Tzu et al. and Lee do not

disclose that the third pattern is positioned on the center of the main field region, and the transferred third pattern on the circuit region of the semiconductor wafer is employed to perform the phase angle test and the transparency test.

Referring to claim 8 and claim 17, Hasegawa et al., Tzu et al. and Lee do not disclose that either the second pattern or the third pattern comprises a cross-shaped pattern composed of the mask substrate and the phase shift layer.

Claims 2-12 are dependent upon the amended claim 1, and claims 14-20 are dependent upon the amended claim 13. Therefore, they should be allowable if claims 1 and 13 are allowable. Reconsideration of claims 2-12 and claims 14-20 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)